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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,277	01/17/2002	Jensen Hartrung Jensen	US028005	4820

7590 06/22/2004

Corporate Patent Counsel
U.S. Philips Corporation
580 White Plains Road
Tarrytown, NY 10591

EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	3

DATE MAILED: 06/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/052,277	Applicant(s) JENSEN, JENSEN HARTRUNG	
	Examiner Christopher E. Lee	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

a) Substitute "the interface 320" by --the interface 125--.

b) In lines 16-17 on page 7, the text disclosure recites "the enable-override gate 220 may be included in each target interface 125". However, the reference symbol 220 is not referring to the enable-override gate, and each target interface does not include the enable-override gate (See Fig. 2). Appropriate correction is required.

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the specification fails to provide the claimed limitation "the bus controller includes one or more devices that operate in dependence up the enabling signal" in lines 2-3 of the claim 8 under a proper antecedent basis.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference character(s) mentioned in the description: the reference symbol 230 on page 7, lines 9 and 16 is not in the drawings.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. However, the limitation "the bus controller includes one or more devices that operate in dependence up to the enabling signal" in lines 2-3 of the claim 8 is not shown in the drawings. Therefore, the limitation must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 8 and 9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

In the claim 8, it recites the limitation "the bus controller includes one or more devices that operate in dependence up the enabling signal" in lines 2-3. However, in the prior claims 1 and 7, they recite the limitations (1) "an activity detector that is configured to detect an initiation of a data-transfer operation and to provide therefrom an enabling signal" in lines 5-6 of the claim 1, and (2) "a bus controller that is configured to establish a communication path" in line 1, respectively. Therefore, the claimed subject matter "bus controller" cannot include any device that operates in dependence up the enabling signal because said activity detector detects an initiation of a data-transfer operation on an established communication path by said bus controller and provides therefrom an enabling signal.

The Examiner doubts how the devices included in said bus controller could operate in dependence up said enabling signal for establishing said communication path, since (1) said activity detector cannot detect an initiation of a data-transfer operation before establishing communication path by said bus controller, and thus (2) said activity detector cannot provide therefrom said enabling signal.

Therefore, the claim 8 contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains to make and/or use the invention.

In the specification, paragraph [0016], the Application discloses that an initiator of the plurality of initiators is configured to provide a pre-notification signal, which is different from the initiation signal of a data-transfer operation, to the activity detector before it communicates command or data information to the bus. However, the claim 9 recites that a component (i.e., initiator) of the plurality of components (i.e., initiators) is configured to signal the initiation of the data-transfer operation, which is not the pre-notification signal, to the activity detector before the component (i.e., initiator) initiates the data-transfer operation via the bus structure.

The Examiner doubts how the component is configured to signal the initiation of the data-transfer operation before the component actually initiates the data-transfer operation via the bus structure. In other words, the component should initiate the data-transfer operation in order to signal the initiation of the data-transfer operation via the bus structure to the activity detector.

Therefore, the claim 9 contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains to make and/or use the invention.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 14 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A broad range or limitation together with a narrow range or limitation that falls within the broad range or limitation (in the same claim) is considered indefinite, since the resulting claim does not clearly set forth the metes and bounds of the patent protection desired. Note the explanation given by the Board of Patent Appeals and Interferences in *Ex parte Wu*, 10 USPQ2d 2031, 2033 (Bd. Pat. App. & Inter. 1989), as to where broad language is followed by "such as" and then narrow language. The Board stated that this can render a claim indefinite by raising a question or doubt as to whether the feature introduced by such language is (a) merely exemplary of the remainder of the claim, and therefore not required, or (b) a required feature of the claims. Note also, for example, the decisions of *Ex parte Steigewald*, 131 USPQ 74 (Bd. App. 1961); *Ex parte Hall*, 83 USPQ 38 (Bd. App. 1948); and *Ex parte Hasche*, 86 USPQ 481 (Bd. App. 1949).

In the present instance, the claim 14 recites the broad recitation the limitation "the enabling of the bus interface is independent of establishing the communications path" in line 2, and the claim also recites the limitation "enabling the bus interface at the target component within a time duration required to establish the communication path" in lines 4-5 of the prior claim 13, which is the narrower statement of the range/limitation because said enabling the bus interface is dependent of establishing the communications path in timewise.

The claim 18 recites the limitation "the completion of the data-transfer operations" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim. Therefore, the term "the completion of the data-transfer operations" could be considered as --a completion of the data-transfer operations-- since it is not clearly defined in the claims.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-7, 10-13 and 15-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Mitchell et al. [US 5,987,614 A; hereinafter Mitchell].

Referring to claim 1, Mitchell discloses a system (i.e., distributed power management system; See col. 1, lines 5-10) comprising: a plurality of components (i.e., CPU 40, Subsystem 1, ... Subsystem n in Fig. 3), a bus structure (i.e., Data 71, Address 72, Bus controls & status 73, Bus clock 74, Power down 75 and Central bus interface 43 in Fig. 3) that is configured to facilitate communications among said plurality of components (See col. 7, lines 39-54), and an activity detector (i.e., Address Comparison Logic 92 and Clock Control Gate Logic 53 in Fig. 4) that is configured to detect an initiation of a data-transfer operation (See col. 7, lines 43-46 and 55-57; i.e., detecting a particular bus cycle) and to provide therefrom an enabling signal (i.e.,

gbclk 57a of Fig. 3) that is communicated to a bus interface (i.e., core logic 1 52a of Fig. 3) of at least one of said plurality of components (i.e., CPU, Subsystem 1, ... Subsystem n), wherein said bus interface (i.e., core logic 1) is configured to be enabled to receive data from said bus structure upon receipt of said enabling signal from said activity detector (See col. 7, line 59 through col. 8, line 3).

Referring to claim 2, Mitchell teaches said activity detector (i.e., Address Comparison Logic 92 and Clock Control Gate Logic 53 in Fig. 4) is configured to detect a completion of said data-transfer operation (See col. 8, lines 3-5; i.e., detecting a completion of the particular bus cycle), and terminates said enabling signal (i.e., gbclk 57a of Fig. 3) based on said completion of said data-transfer operation (See col. 8, lines 5-6), and said bus interface (i.e., core logic 1) is configured to be disabled from receiving data from said bus structure upon termination of said enabling signal (See col. 8, lines 6-8).

Referring to claim 3, Mitchell teaches said enabling signal (i.e., gbclk 57a of Fig. 3) includes a gated clock signal (i.e., gbclk 67 from control gate logic 63 in Fig. 7).

Referring to claim 4, Mitchell teaches said bus interface (i.e., core logic 1 52a of Fig. 3) includes a plurality of clocked devices (i.e., color fill engine 504, EDO DRAM 502, SDRAM 503, etc. in Fig. 6) that are clocked based on said enabling signal (i.e., being clocked by gbclk 57a of Fig. 3).

Referring to claim 5, Mitchell teaches said activity detector (i.e., Address Comparison Logic 92 and Clock Control Gate Logic 53 in Fig. 4) includes: a set-reset device (i.e., Flip-Flop 106 of Fig. 7) that is set (i.e., en^+ appearance from Flip-Flop 106 in Fig. 7) upon detection of said initiation of said data-transfer operation (See col. 7, lines 55-57 and col. 13, lines 47-58), and a delay device (i.e., Flip-Flop 107 of Fig. 7), operably coupled to said set-reset device (See col. 14, lines 7-12), that is configured to provide said enabling signal (i.e., gbclk 67 of Fig. 7) synchronous with a system clock (i.e., gbclk is synchronized with bus clock bclk in Fig. 8) that is

common to said bus structure (i.e., bus system clock; See col. 7, lines 38-43), based on whether said set-reset device is set (See col. 13, lines 56-60).

Referring to claim 6, Mitchell teaches said set-reset device (i.e., Flip-Flop 106 of Fig. 7) is reset (i.e., en^+ disappearance from Flip-Flop 106 in Fig. 7) upon detection of a completion of said data-transfer operation (See col. 8, lines 3-8 and col. 13, lines 58-60).

Referring to claim 7, Mitchell teaches a bus controller (i.e., Address Decode Logic 91 and Address Comparison Logic 92 in Fig. 4) that is configured to establish a communications path (See col. 18, lines 3-25 and Fig 16) between an initiating component (i.e., CPU 40 or any Subsystem requesting resources on a target Subsystem in Fig. 3) of said plurality of components (i.e., CPU 40, Subsystem 1, ... Subsystem n in Fig. 3) and a target component (e.g., Subsystem 1 51 in Fig. 3) of said plurality of components, wherein said activity detector (i.e., Address Comparison Logic 92 and Clock Control Gate Logic 53 in Fig. 4) provides said enabling signal (i.e., gbclk 57a of Fig. 3) within a time duration consumed by said bus controller to establish said communications path (i.e., the time duration for establishing communication path from CPU to Subsystem 1 is longer than the time duration for providing the enabling signal because the communication path should be established after the activity detector generates the enabling signal, which clearly anticipates said activity detector providing said enabling signal within a time duration consumed by said bus controller to establish said communications path; See col. 7, line 38 through col. 8, line 3 and Fig. 3).

Referring to claim 10, Mitchell discloses a method of reducing power consumption in a system (i.e., distributed power management system; See col. 3, lines 66-67) comprising a plurality of components (i.e., CPU 40, Subsystem 1, ... Subsystem n in Fig. 3) that are configured to communicate via a bus structure (i.e., Data 71, Address 72, Bus controls & status 73, Bus clock 74, Power down 75 and Central bus interface 43 in Fig. 3; See col. 7, lines 39-54), comprising: detecting an initiation of bus activity (i.e., accessing resources via a bus) by a component of said

plurality of components (See col. 7, lines 43-46 and 55-57; i.e., detecting a particular bus cycle requiring resources within a subsystem of the plurality of components by one of the plurality of components, e.g., CPU), communicating an enabling signal (i.e., gbclk 57a of Fig. 3) to one or more other components of said plurality of components (e.g., Subsystem 1 51 in Fig. 3), and enabling a bus interface (i.e., core logic 1 52a of Fig. 3) at each of said one or more other components (i.e., Subsystem 1) to receive signals corresponding to said bus activity, based on said enabling signal (See col. 7, line 59 through col. 8, line 3).

Referring to claim 11, Mitchell teaches detecting a completion of said bus activity (See col. 8, lines 3-5; i.e., detecting a completion of the particular bus cycle), and disabling said bus interface at each of said one or more other components, based on said completion of said bus activity (See col. 8, lines 5-8).

Referring to claim 12, Mitchell teaches synchronizing (i.e., gbclk is synchronized with bus clock bclk in Fig. 8) said enabling signal (i.e., gbclk 67 of Fig. 7) to a system clock (i.e., bclk 74 of Fig. 7) that is common to said bus structure (i.e., bus system clock; See col. 7, lines 38-43).

Referring to claim 13, Mitchell teaches establishing a communications path (See col. 18, lines 3-25 and Fig 16) between said component that initiated said bus activity (i.e., CPU 40 or any Subsystem requesting resources on a target Subsystem in Fig. 3) and a target component (e.g., Subsystem 1 51 in Fig. 3) of said one or more other components, and enabling said bus interface (i.e., core logic 1 52a of Fig. 3) at said target component within a time duration required to establish said communications path (i.e., the time duration for establishing communication path from CPU to Subsystem 1 is longer than the time duration for enabling said bus interface because the communication path should be established after the activity detector generates the enabling signal, which clearly anticipates the step of enabling said bus interface at said target component within a time duration required to establish said communications path; See col. 7, line 38 through col. 8, line 3 and Fig. 3).

Referring to claim 15, Mitchell discloses an electronic circuit (i.e., distributed power management system; See col. 1, lines 5-10) comprising: a plurality of initiators (i.e., Subsystem 1, ... Subsystem n in Fig. 3) that are configured to selectively initiate data-transfer operations (i.e., requesting resources which are included in target; See col. 7, lines 47-54) via a bus structure (i.e., Data 71, Address 72, Bus controls & status 73, Bus clock 74, Power down 75 and Central bus interface 43 in Fig. 3), a plurality of targets (i.e., Subsystem 1, ... Subsystem n in Fig. 3) that are configured to process said data-transfer operations (i.e., providing requested resources; See col. 7, lines 55-61), each of said plurality of targets (e.g., Subsystem 1 51 in Fig. 3) including an interface (i.e., core logic 1 52a of Fig. 3) for receiving said data-transfer operations, and an activity detector (i.e., Address Comparison Logic 92 and Clock Control Gate Logic 53 in Fig. 4) that is configured to detect an initiation of a data-transfer operation from any of said plurality of initiators (See col. 7, lines 43-46 and 55-57; i.e., detecting a particular bus cycle), and to generate therefrom an enabling signal (i.e., gbclk 57a of Fig. 3), wherein said interface (i.e., core logic 1) of each of said plurality of targets is configured to receive said data-transfer operations in dependence upon said enabling signal from said activity detector (See col. 7, line 59 through col. 8, line 3).

Referring to claim 16, Mitchell teaches said plurality of initiators (i.e., Subsystem 1, ... Subsystem n in Fig. 3) are configured to effect said data-transfer operations at a system clock speed (i.e., bus clock bclk in Fig. 8; in fact, all the Subsystems are operating under the system bus clock bclk 74 in Fig. 3), and said interface (i.e., core logic 52 in Fig. 3) of each of said plurality of targets is configured to operate at said system clock speed (i.e., bclk speed in Fig. 8) only when said activity detector (i.e., Address Comparison Logic 92 and Clock Control Gate Logic 53 in Fig. 4) provides said enabling signal (i.e., gbclk 57 of Fig. 3; See col. 13, line 40 through col. 14, line 13).

Referring to claim 17, Mitchell teaches said enabling signal (i.e., gbclk 57a of Fig. 3) includes a clocking signal that operates at said system clock speed (i.e., a gated clock signal gbclk 67 from control gate logic 63 in Fig. 7).

Referring to claim 18, Mitchell teaches said activity detector is configured to detect a completion of said data-transfer operations (See col. 8, lines 3-5; i.e., detecting a completion of the particular bus cycle), and to terminate said generation of said enabling signal (i.e., disabling gbclk 57a of Fig. 3) based on said completion of said data-transfer operations (See col. 8, lines 5-8).

Referring to claim 19, Mitchell teaches a bus controller (i.e., Address Decode Logic 91 and Address Comparison Logic 92 in Fig. 4) that is configured to establish a communications path (See col. 18, lines 3-25 and Fig 16) between an initiator of said plurality of initiators (i.e., any one of Subsystems requesting resources on a target Subsystem in Fig. 3) and a target (e.g., Subsystem 1 51 in Fig. 3) of said plurality of targets, wherein said activity detector (i.e., Address Comparison Logic 92 and Clock Control Gate Logic 53 in Fig. 4) is configured to generate said enabling signal (i.e., gbclk 57a of Fig. 3) within a time duration required by said bus controller to establish said communications path (i.e., the time duration for establishing communication path from CPU to Subsystem 1 is longer than the time duration for providing the enabling signal because the communication path should be established after the activity detector generates the enabling signal, which clearly anticipates said activity detector is configured to generate said enabling signal within a time duration required by said bus controller to establish said communications path; See col. 7, line 38 through col. 8, line 3 and Fig. 3).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Minami et al. [US 6,272,667 B1] disclose method and apparatus for clock gated logic circuits to reduce electric power consumption.

Watabiki et al. [JP 409106383 A] disclose bus switching device.

12. The Examiner refers to Watabiki et al. [JP 409106383 A] reference as a prior art made of record and not relied upon in the instant Office Action, and it is referred to the original copy of foreign reference in foreign language (i.e., Japanese). The Examiner attaches a machine translated copy of the reference for the convenience of the Applicant(s). However, the Examiner cautions the Applicant(s) that the Office is not responsible for any erroneous interpretation resulting from inaccuracies between the original foreign language reference and the machine translation of the reference, as the machine translation may not reflect the original precisely.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Examiner
Art Unit 2112

cel/ CEL

Glenn A. Auve
Primary Patent Examiner
Technology Center 2100